AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1.(currently amended) A nonvolatile semiconductor memory device comprising:

a memory cell array in which plural nonvolatile memory cells are arranged in matrix,

a connection ~~portions~~portion for an active ~~regions~~region that partially ~~connect~~connects first and second active regions adjacent with each other with a device isolation region ~~of the memory cell array~~ put therebetween in a first direction in which control gates extend in the memory cell array,

a contact ~~holes~~hole for connecting a global bit ~~lines~~line to the connection ~~portions~~portion, ~~and~~

~~first and second selection transistors disposed each by one on the first and second active regions for selecting the first and second active regions~~

a first selection transistor for selecting the first active region disposed between the contact hole and the memory cell array, and a second selection transistor for selecting the second active region disposed between the contact hole and the memory cell array.

2. (currently amended) A nonvolatile semiconductor memory device according to claim 1, wherein gates of the first and second selection transistors for selecting the first and second active regions are separated, and the gate of the first transistor and the gate of the second transistor are disposed without overlap thereof along the first direction.

3. (original) A nonvolatile semiconductor memory device according to claim 2, wherein the separated gates of the first and second selection transistors are arranged in two stages in the direction of the global bit line.

4. (original) A nonvolatile semiconductor memory device according to claim 3, wherein the gates for the selection transistor in each stage are disposed on every other active region.

5. (original) A nonvolatile semiconductor memory device according to claim 2, wherein the contact hole is

formed about at an intersection between one of the first and second active regions and the connection portion, and one of the gates of the first and second selection transistors that is disposed on the side of the memory cell is disposed on the active region in which the contact hole is formed.

6. (original) A nonvolatile semiconductor memory device according to claim 5, wherein the gate for the first and second selection transistors is separated and disposed being further extended from the first active region to the third active region adjacent with the second active region.

7. (original) A nonvolatile semiconductor memory device according to claim 2, wherein the gates of the selection transistors and the memory blocks constituting the memory cell array are disposed in mirror symmetry with respect to a plane perpendicular to the global bit line and passing through the connection portion for the active regions.

8. (original) A nonvolatile semiconductor memory device according to claim 2, wherein the memory blocks constituting the memory cell array are disposed in mirror symmetry with respect to a plane perpendicular to the global

bit line and passing through the connection portion for the active regions, while the gates of the selection transistors are disposed in mirror asymmetry with respect to the plane perpendicular to the global bit line and passing through the connection portion for the active regions.

9. (original) A nonvolatile semiconductor memory device according to claim 2, wherein the memory cells are connected in series with the direction of the global bit line.

10. (original) A nonvolatile semiconductor memory device according to claim 2, wherein the memory cells are connected in parallel with the direction of the global bit line.

11. (original) A nonvolatile semiconductor memory device according to claim 2, wherein the nonvolatile memory cell has a first gate, a second gate, and a third gate different in the function from the first gate and the second gate.

12. (currently amended) A nonvolatile semiconductor memory device comprising a memory cell array constituted by

arranging, in a matrix, nonvolatile memory cells each having a first gate, a second gate, and a third gate different in the function from the first gate and the second gate, in which two active regions adjacent to each other with the device isolation region ~~of the memory cells~~ put therebetween in a first direction in which control gates extend are combined in one set, and respective active regions are connected by way of contact holes to a global bit line in common, and having first and second selection transistors for selecting the active regions.

13. (new) A nonvolatile semiconductor memory device according to claim 12, wherein the gate of the first selection transistor and the gate of the second selection transistor are disposed without overlap thereof along the first direction.

14. (new) A nonvolatile semiconductor memory device according to claim 2, wherein the distance in a second direction across the first direction between the gate of the first selection transistor and the gate of the second selection transistor is within a minimum fabrication size.

15. (new) A nonvolatile semiconductor memory device according to claim 13, wherein the distance in a second direction across the first direction between the gate of the first selection transistor and the gate of the second selection transistor is within a minimum fabrication size.

16. (new) A nonvolatile semiconductor memory device comprising:

a memory cell array having a control gate extending in a first direction in a memory cell region,

a first active region and as second active region adjacent in the first direction, formed in a selection transistor region and extending up to the memory cell region,

a connection region to connect a part of the first active region and a part of the second active region,

a first selection transistor for selecting any memory cell disposed on the first active region, and

a second selection transistor for selecting any memory cell disposed on the second active region, and

wherein a gate of the first selection transistor and a gate of the second selection transistor are disposed without overlap thereof along the first direction and a second direction perpendicular to the first direction.

17. (new) A nonvolatile semiconductor memory device according to claim 16, wherein the distance in the second direction between the gate of the first selection transistor and the gate of the second selection transistor is within a minimum fabrication size.